CLAIMS

What is claimed is:

1. A method, comprising the acts of:
   (a) measuring values associated with a plurality of memory elements, wherein the values are indicative of a digital state;
   (b) calculating a plurality of terms associated with transitions in the values between memory elements; and
   (c) determining the digital state of at least one memory element using the calculations from (b).

2. The method of claim 1, wherein act (b) comprises calculating the plurality of terms between proximate memory elements.

3. The method of claim 2, wherein the proximate memory elements have observed values that vary due to processing inefficiencies.

4. The method of claim 2, wherein the calculations comprise calculating a sum of terms associated with transitions.

5. The method of claim 4, wherein act (c) comprises determining the digital states of a memory word by choosing an outcome that minimizes the sum of transition-terms.

6. The method of claim 2, further comprising initializing the plurality of memory elements to limit the length of repetitive digital states.

7. The method of claim 6, wherein initialization includes allocating at least one additional memory element.

8. The method of claim 6, wherein initialization includes encoding the plurality of memory elements.

9. The method of claim 1, wherein the memory elements comprise magnetic memory elements.

10. The method of claim 9, wherein the values measured in (a) represent resistive values.

11. A memory, comprising:

a plurality of memory elements;

circuitry coupled to the plurality of memory elements; and

wherein the circuitry observes values of a plurality of memory elements corresponding to digital states, and utilizes the observed values to determine the digital state of at least one memory element.

12. The memory of claim 11, wherein the observed values are used to calculate a plurality of transition-terms associated with possible transitions between proximate memory elements.

13. The memory of claim 12, wherein the proximate memory elements have observed values that vary due to processing inefficiencies.

14. The memory of claim 11, wherein the circuitry includes a comparison device and a register.

15. The memory of claim 14, wherein the comparison device compares the contents of the register to determine the digital state of a desired memory element.

16. The memory of claim 15, wherein the contents of the register represent an adaptive threshold that is modified to reflect previous determinations of previous memory elements.

17. The memory of claim 12, wherein the plurality of transition-terms are used to determine the digital state of a memory word.

18. The memory of claim 17, wherein the plurality of memory elements are initialized to limit the length of repetitive digital states.

19. The method of claim 18, wherein initialization includes allocating at least one additional memory element.

20. The memory of claim 18, wherein initialization includes encoding the data using an $8/9^{ths}$ code, in which an 8 bit data word is encoded as a 9 bit code word.

21. The method of claim 11, wherein the memory elements comprise magnetic memory elements.

22. The method of claim 21, wherein the observed values represent resistive values.

23. A computer, comprising:

a processor;

a memory coupled to the processor, wherein the memory further comprises a plurality of memory elements;

circuitry coupled to the plurality of memory elements; and

wherein the circuitry observes values of a plurality of memory elements corresponding to digital states, and utilizes the values of proximate memory elements to predict the digital state of at least one memory element.

24. The memory of claim 23, wherein the circuitry includes a comparison device and a register.

25. The memory of claim 24, wherein the comparison device compares the contents of the register to determine the digital state of a desired memory element.

26. The memory of claim 25, wherein the contents of the register represent an adaptive threshold that is modified to reflect previous determinations of previous memory elements.

27. The computer of claim 23, wherein the values are used to calculate a plurality of transition-terms associated with the possible transitions between proximate memory elements.

28. The memory of claim 27, wherein the proximate memory elements have observed values that vary due to processing inefficiencies.

29. The computer of claim 27, wherein the plurality of transition-terms are used to determine the digital state of a memory word.

30. The computer of claim 23, wherein the memory elements comprise magnetic memory elements.

31. The computer of claim 30, wherein the values observed represent resistive values.

32. A method, comprising:

(a) comparing values of a plurality of memory elements to an adaptive threshold, wherein the values are indicative of a digital state;

(b) determining the digital state indicated by the comparison of (a); and

(c) updating the adaptive threshold to include the compared value and its digital state.

33. The method of claim 32, wherein the adaptive threshold represents an average of the plurality of values for proximate memory elements.

34. The method of claim 33, wherein the memory elements comprise magnetic memory elements.

35. The method of claim 34, wherein the values compared in (a) represent resistive values.

36. The memory of claim 34, wherein the proximate memory elements have resistances that vary due to processing inefficiencies.

37. The method of claim 35, wherein the adaptive threshold is initialized using a resistive reference.

38. A memory, comprising:
a plurality of memory elements;
comparison circuitry coupled to the plurality of memory elements;
a register coupled to the comparison circuitry; and
wherein the comparison circuitry compares values of the plurality of memory elements to an adaptive threshold contained in the register, determines a digital state indicated by the comparison, and updates the adaptive threshold contained in the register to include the values for the indicated digital state.

39. The memory of claim 38, wherein the adaptive threshold represents an average of the plurality of values for proximate memory elements.

40. The memory of claim 39, wherein the proximate memory elements have observed values that vary due to processing inefficiencies.

41. The memory of claim 39, wherein the plurality of memory elements comprise magnetic memory elements.

42. The memory of claim 41, wherein the values compared represent resistive values.

43. The memory of claim 42, wherein the adaptive threshold is initialized using at least one resistive reference.

44. A method, comprising:

encoding data into a plurality of proximate memory elements, such that proximate memory elements are compared in order to decode the data; and

decoding the data by comparing proximate memory elements.

45. The method of claim 44, wherein the memory elements comprise magnetic memory elements.

46. The method of claim 45, wherein the memory elements represent resistive values.

47. The memory of claim 46, wherein the proximate memory elements have resistances that vary due to processing inefficiencies.

48. A memory, comprising:

a plurality of memory elements;

circuitry coupled to the plurality of memory elements;

wherein the circuitry writes transition-encoded data into a plurality of proximate memory elements and reads transition-encoded data by comparing the proximate memory elements.

49. The memory of claim 48, wherein the plurality of memory elements comprise magnetic memory elements.

50. The memory of claim 49, wherein the values compared represent resistive values.

51. The memory of claim 50, wherein the proximate memory elements have resistances that vary due to processing inefficiencies.

52. A memory, comprising:

a means for observing values of a plurality of memory elements; and

a means for determining the digital state of at least one memory using measured values of proximate memory elements.